

## REMARKS

The Specification has been amended to reference the PCT Application and the United Kingdom Patent from which this application claims priority.

The disclosure was objected to for not including a header for the background of the invention. Page 1 of the disclosure has been amended to insert this header. Therefore, this objection should be withdrawn.

The examiner objected to the drawings for failing to include reference characters not mentioned in the description. The description has been amended to include the relevant labels for Figure 5, 10 and 11. More specifically, the first paragraph of page 7 has been amended to include reference to the OPA 602 buffers and the output number 6 of the first AD844 chip. The paragraph beginning at page 8, line 29 has been amended to include reference to the buffer IC1 and further reference to the passive components C1, R1, R2, and R3. The paragraph has also been amended at page 9 to include other references used as the labels in Figure 11. It is believed that no new matter has been added by mention of the labels in the specification. Therefore, the objections to the drawings should be withdrawn.

Claims 20-22 were objected to because of the format of the preambles for these claims. Claims 2-22 have been amended to recite “The system as claimed in...” Therefore, this objection should be withdrawn.

Claims 4, 7, 8, and 12-22 were rejected under §112, second paragraph as being indefinite for a number of reasons. Claim 4 has been amended to delete the phrase “preferably via an IEEE 1394 Interface”. As noted by the Examiner, use of this interface is not critical or inherent. Claim 7 has been amended to recite that the plurality of digital signal processing modules comprises four digital signal processing modules, thereby providing an antecedent basis for the reference to the third digital signal processing module. Similarly, in claim 8, this amendment provides antecedent basis for recitation of the fourth digital signal processing module.

Claim 12 has been amended to delete the terms “or equivalents”. Claim 11 has been revised to recite that the data acquisition systems each includes a voltage controlled current source, equal width pulse synthesizer, and a synchronized digital demodulation unit in order to provide the proper antecedent basis for the claims 12-22. Claim 12 has been amended to also recite that the two inverting inputs of each pair are connected together, rather than being

cascaded together. Page 7 of the description has been amended consistent with the claim 12 noting that Figure 5 clearly shows the inputs being connected together with the resistor.

Claims 13 and 14 have been amended to refer to the negative and positive current outputs of the four pairs of AD 844 chips, consistent with the reference in claim 12 in which claims 13 and 14 depend, to the eight AD 844 chips configured as four pairs.

Claim 15 has been amended to recite that the DC restore facility restores DC components generated in the system and cancels a DC offset at the current outputs of the AD 844 chips. Page 7, lines 1-3 provide a description of this limitation. Claim 15 has been further amended to recite the connection of the capacitor and resistor in relation to the OPA 602 chip shown in the Figure 5. Amended claim 15 clearly defines that the arrangement of the DC restore facility restores the DC components generated, and cancels the offset at the current outputs of the AD 844 chips.

Claim 17 has been amended to recite that the equal with pulse synthesizer has different sampling rates at different frequencies so that the staircase signal output has the same time step-length at all frequencies. Support for this description is found on page 7, line 25 in which the invention is clearly defined such that the EWPS has different sampling rates at the different signal frequencies such that the staircase signal output has the same time step-length at all frequencies. Further, claim 17 avoids use of the terms “are provided”.

Claim 19 has been amended to recite that the demodulation unit comprises 16 programmable gain amplifiers each having an analog to digital converter, two strobed FIFO memories, and control logic. Claim 19 has been further amended to delete the terms “sets of”.

Claim 22 has been amended to recite the reference to the DE type flip-flop that prevents data being written prematurely to the second of the flip-flops. As recognized by the Examiner, since operation of the D type flip-flop is inherent, it is believed that the deleted language in this claim was redundant. Therefore, the rejection under §112 should be withdrawn.

Claim 26 was rejected under §101 as being directed to non-statutory subject matter. Pursuant to the Examiner’s suggestion, Claim 26 has been revised to recite that the invention is drawn to a non-transitory computer readable medium. Therefore, this rejection under §101 should be withdrawn.

Claims 1-11, 24 and 26 were rejected under §102 as being anticipated by Bai. Claim 1 has been amended to recite a number of additional features to include at least one of the data acquisition sub-systems including an over-zero switch comprising at least one multiplexor and at

least one flip-flop, and further recites details of the flip-flop receiving a synchronization signal having the same over-zero point as a sinusoidal signal, the synchronization signal causing the at least one flip-flop to output a channel selection signal provided to the flip-flop. These features are not remotely disclosed in the Bai reference.

Based at least upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,  
SHERIDAN ROSS P.C.

By: /Brent P. Johnson/  
Brent P. Johnson  
Registration No. 38031  
1560 Broadway, Suite 1200  
Denver, Colorado 80202-5141  
(303) 863-9700

Date: January 24, 2011